

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1491	(703/28.ccls. 714/28.ccls. 714/29.ccls. 714/30.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:35
L2	110	(microcontroller same (fpga emulat\$4) same (lock\$step synchroniz\$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:35
L3	21	((lock\$step) same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:37
L4	145	(ice same emulat\$5) and (compare with (register memory content))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:38
L5	21	((master and slave) same (microcontroller)) same (compar\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:42
L6	5067	((parallel lock\$step) same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:44
L7	56	L6 and "703".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:45
L8	243	L6 and "714".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:45
L9	219	8 not 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/07 14:45

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L10	4	(microcontroller and (emulator emulation) and (synchronization synchronized lock\$step synchronous)).clm.	US-PGPUB	OR	ON	2007/11/07 14:51
L11	33	((processor cpu microprocessor) and (emulator emulation) and (synchronization synchronized lock\$step synchronous)).clm.	US-PGPUB	OR	ON	2007/11/07 14:53
L12	106	((processor cpu microprocessor microcontroller) and (emulator emulation simulator simulation) and (breakpoint halt debug)).clm.	US-PGPUB	OR	ON	2007/11/07 14:54
L13	14	((processor cpu microprocessor microcontroller) and (emulator emulation simulator simulation) and (breakpoint halt debug) and (lock\$step synchronous synchronized synchronization)).clm.	US-PGPUB	OR	ON	2007/11/07 14:55
L14	0	13 not 12	US-PGPUB	OR	ON	2007/11/07 14:55
L15	92	12 not 13	US-PGPUB	OR	ON	2007/11/07 15:18

*PGPub Interference
Search 11/7/2007
JMP*